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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER
LIU, BEN H

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,239	BROWN ET AL.	
	Examiner	Art Unit	
	Ben H. Liu	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *November 20. 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to an amendment/response filed on November 20, 2007.

2. No claims have been cancelled.

3. No claims have been added.

4. Claims 1-22 are currently pending.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. For claim 18, the claimed invention is directed to non-statutory subject matter. The claim is directed to "an article of manufacture comprising a machine-readable storage medium." The claim fails to mention a a computer readable medium encoded with, stored with, or embodied with computer executable instructions. Without these components the functionality of the claimed invention cannot be carried out.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3, 5, 8-10, 13-14, 16-19, and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Amit (U.S. Patent 7,197,045).

For claims 1 and 17-19, Amit discloses a processor comprising at least a portion of a first split transmit and receive media access controller, the split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another *(see column 2 lines 28-33, which recite separated MAC receivers and transmitters)*; wherein an interface for directing signals between the transmit unit and the receive unit of the first split transmit and receive media access controller is configurable to multiplex the signals with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller *(see figure 6 and column 2 lines 43-47, which recite a switch interface that is coupled to the MAC receivers and transmitters)*.

For claims 3, 21 and 22, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein one or more of the transmit units are implemented on a first integrated circuit and one or more of the receive units are implemented on a second integrated circuit *(see column 2 lines 34-42)*.

For claim 5, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein the interface comprises a receive interface block coupled to a generate interface block via an interface bus, the generate interface block receiving signals from a plurality of media access controller receive units and multiplexing the signals onto the interface bus for delivery to

the receive interface block, the receive interface block demultiplexing the signals from the interface bus for delivery to appropriates ones of a plurality of media access controller transmit units *(see column 5 lines 28-45, which recite a switch 352 that multiplexes signals from multiple MAC receivers and de-multiplexes the signals for delivery to a plurality of MAC transmitters).*

For claim 8, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein the interface bus comprises a separate dedicated information signal bus for delivering carrier sense signals between one or more of the receive units and one or more of the transmit units in an internal mode of operation of the interface *(see column 5 lines 20-27, which recite the switch interface 352 as an Ethernet switch. The Ethernet protocol employs carrier sense multiple access that delivers a carrier signal to indicate impending transmission).*

For claim 9, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein the signals received by the generate interface block for delivery to the receive interface block comprise one or more of carrier sense signals, auto-negotiation signals, flow control signals, and deference reset signals *(see column 5 lines 20-27, which recite the switch interface 352 as an Ethernet switch. The Ethernet protocol employs carrier sense multiple access that delivers a carrier signal to indicate impending transmission).*

For claim 10, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein the signals received by the generate interface block are multiplexed onto the interface bus using a priority-based selection mechanism which assigns the highest priority to the carrier

sense signals, the second highest priority to the auto-negotiation signals, and lower priorities to the flow control and deference reset signals *(see column 6 lines 10-14)*.

For claim 13, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein the interface comprises a plurality of channels, each having one or more ports associated therewith, and wherein a given signal to be directed between transmit and receive units of a given split transmit and receive media access controller is assigned to a particular channel and port of the interface *(see column 6 lines 43-47)*.

For claim 14, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein each of the channels may have up to eight ports, with a single-bit nibble address being utilized to identify a particular one of first and second four-port groups of a given eight-port channel *(see column 6 lines 43-47)*.

For claim 16, Amit discloses a processor comprising a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another wherein the processor comprises a network processor *(see figure 6)*.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 2, 4, 7, 11, 12, 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amit (U.S. Patent 7,197,045) in view of Wakeman et al. (U.S. Patent 5,790,786).

For claims 2, 4, 15, and 20, Amit et al. discloses all the subject matter of the claimed invention with the exception wherein one or more of the transmit units are implemented in a first region of an integrated circuit, and one or more of the receive units are implemented in a second

region of the integrated circuit, remote from the first region as recited in claims 2 and 20; wherein the interface is configured to deliver signals between one or more transmit units and one or more receive units where the transmit units and the receive units are implemented on the same integrated circuit as recited in claim 4; and wherein the processor comprises an integrated circuit as recited in claim 15.

Wakeman et al. from the same or similar fields of endeavor teach a portion of a media access controller including a plurality of receive data path units that are multiplexed to a plurality of transmit data path units *(see column 2 lines 34-46)*. The separate transmit data path units and receive data path units are located on a single integrated circuit *(see column 3 lines 7-12)*. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the plurality of receive data path units that are multiplexed to a plurality of separate transmit data path units located on different portions of an integrated circuit as taught by Wakeman et al. with the processor including a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another as taught by Amit. The plurality of receive data path units that are multiplexed to a plurality of separate transmit data path units can be implemented by combining the transmit and receive controllers and data paths as taught by Wakeman et al. in the integrated circuit of the first or second MAC function taught by Amit. The motivation for using the plurality of receive data path units that are multiplexed to a plurality of separate transmit data path units in the integrated circuit of the first or second MAC function is to improve the efficient use of integrated circuit space.

For claim 7, Amit et al. discloses all the subject matter of the claimed invention with the exception wherein the interface bus comprises a five-bit wide information signal bus and at least

one clock signal line. Wakeman et al. from the same or similar fields of endeavor teach a portion of a media access controller including a plurality of receive data path units that are multiplexed to a plurality of transmit data path units *(see column 2 lines 34-46)*. The plurality of receive data path units are multiplexed to a plurality of transmit data path units through a bus interface unit *(see figure 2a)*. The plurality of receive data path units and plurality of transmit data path units also receive clocking signals such as RXC *(see figure 5b and column 9 lines 8-11)*. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use plurality of receive data path units are multiplexed to a plurality of transmit data path units through a bus interface unit as taught by Wakeman et al. with the processor including a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another as taught by Amit. The plurality of receive data path units are multiplexed to a plurality of transmit data path units through an interface bus can be implemented by coupling the bus interface unit as taught by Wakeman et al. with the transmit unit and receive unit as taught by Amit. The motivation for using the bus interface unit as taught by Wakeman et al. with the split transmit and receive media access controller processor as taught by Amit is to allow traffic from the receive units to be sent to sent the transmit units.

For claims 11 and 12, Amit et al. discloses all the subject matter of the claimed invention with the exception wherein the interface operates in accordance with a state machine having at least a synchronization state, a control address state and one or more data states as recited in claim 11 and wherein the control address state carries information regarding signal type and signal interface address as recited in claim 12.

Wakeman et al. from the same or similar fields of endeavor teach a portion of a media access controller including a plurality of receive data path units that are multiplexed to a plurality of transmit data path units *(see column 2 lines 34-46)*. The media access controller includes a sequencer which drives a state machine. The state machine receives state, status, and control signals from the sequencer *(see column 3 lines 47-56)*. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the plurality of receive data path units and a plurality of transmit data path units controlled by a state machine as taught by Wakeman et al. with the processor including a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another as taught by Amit. The state machine as taught by Wakeman et al. can be implemented by installing RAM containing state and count signals corresponding to the state machine in the split transmit and receive media access controller processor as taught by Amit. The motivation for using the state machine as taught by Wakeman et al. with the split transmit and receive media access controller processor as taught by Amit is to enable monitoring and controlling of the various transmit and receive units.

13. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Amit (U.S. Patent 7,197,045) in view of Appala et al. (U.S. Patent 6,862,265).

For claim 6, Amit et al. discloses all the subject matter of the claimed invention with the exception wherein the interface block multiplexes the signals onto the interface bus utilizing a plurality of round-robin arbiters. Appala et al. from the same or similar fields of endeavor teach a round robin scheduler that supplies the data frames to the corresponding transmit port *(see*

column 4 lines57-67, column 5 lines 1-3, and figure 2). Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the round robin scheduler that supplies the data frames to the corresponding transmit port as taught by Appala et al. with the processor including a split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another as taught by Amit. The round robin scheduler that supplies the data frames to the corresponding transmit port as taught by Appala et al. can be implemented by coupling the scheduler to the interface for directing signals between the transmit unit and the receive unit of the a split transmit and receive media access processor as taught by Amit. The motivation for using the round robin scheduler that supplies the data frames to the corresponding transmit port as taught by Appala et al. with the split transmit and receive media access controller processor as taught by Amit is to enable prioritized queuing of layer 2 network traffic.

Response to Arguments

14. Upon further consideration, claims 1-22 are not allowable because the limitations are taught by Amit (U.S. Patent 7,197,045) and in view of various cited prior art.

15. Upon further consideration, claims 1-12, even if previously indicated as allowable subject matter if rewritten in independent form including all the limitations of the base claim and any intervening claims, are not allowable because the limitations are taught by various cited prior art.

16. Claim 18 is presently rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

17. Claims 1, 3, 5, 8-10, 13-14, 16-19, and 21-22 are presently rejected under 35 U.S.C. 102(b) as being anticipated by Amit (U.S. Patent 7,197,045).

18. Claims 2, 4, 7, 11, 12, 15 and 20 are presently rejected under 35 U.S.C. 103(a) as being unpatentable over Amit (U.S. Patent 7,197,045) in view of Wakeman et al. (U.S. Patent 5,790,786).

19. Claim 6 is presently rejected under 35 U.S.C. 103(a) as being unpatentable over Amit (U.S. Patent 7,197,045) in view of Appala et al. (U.S. Patent 6,862,265).

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. *(see form PTO-892).*

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben H. Liu whose telephone number is (571) 270-3118. The examiner can normally be reached on 9:00AM to 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on (571) 272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BL

FIRMIN BACKER
SUPERVISORY PATENT EXAMINER